AMENDMENT

In the Claims: **Kindly cancel Claims 1, 5 and 17-20. Kindly amend Claims 2-4 and 6 as follows. No new matter has been introduced.**

2. (Currently amended) A bi-directional amplifier in accordance with Claim ~~1~~6, wherein said first
amplification path is a common source amplifier.

3. (Currently amended) A bi-directional amplifier in accordance with Claim ~~1~~6, wherein said second amplification path is a common source amplifier.

4. (Currently Amended) A bi-directional amplifier in accordance with Claim ~~1~~6, wherein said ~~first mode is a receive mode and said first amplification path is a~~ receiver amplifier ~~which~~ is optimized for low ~~noise further~~ noise, and further comprises ~~comprising~~ a receiver electrode which is biased at a high voltage potential when the receiver amplifier is in the receive mode.

6. (Currently amended) ~~A bi-directional amplifier in accordance with Claim 5, wherein said~~ A bi-directional amplifier having a first mode and a second mode comprising:

a first port;

a second port;

a first amplification path electrically connected between the second port and the first port, biased to directionally couple a signal from the second port to the first port during the first mode and biased off during the second mode;

a second amplification path electrically connected between the first port and the second port, biased to directionally couple a signal from the first port to the second port during the second mode and biased off during the first mode;

said first mode is a receive mode and said first amplification path is a receiver amplifier which further comprises an input matching network and an output matching network for optimizing said receiver amplifier noise figure;

said second mode is a transmit mode and said second amplification path is a transmitter amplifier, which is optimized for high power, further comprising a transmitter electrode that is biased at a high voltage potential when the

transmitter amplifier is in the transmit mode;

said transmitter amplifier further comprises an input matching and output matching network, and said receiver input and output matching networks topologies are asymmetrical to said transmitter input and output matching networks.

7. (Original) A bi-directional amplifier in accordance with Claim 6, wherein said receiver amplifier further comprises interstage matching networks optimized for low noise figure and said transmitter amplifier further comprises interstage matching networks optimized for high power output.

8. (Previously presented) A phased array system comprising:

a plurality of radiating elements;

at least one bi-directional amplifier;

wherein said at least one bi-directional amplifier comprises:

a first port;

a second port;

a receiver amplifier electrically connected between the second port and the first port and optimized for low noise, biased to directionally couple a signal from the second port to the first port during the receive mode and biased off during the transmit mode; and

a transmitter amplifier electrically connected between the first port and the second port and optimized for high power, biased to directionally couple a signal from the first port to the second port during the transmit mode and biased off during the receive mode;

wherein the second port is electrically connected to each radiating element.

9. (Original) A phased array system in accordance with Claim 8, wherein said receiver amplifier is a common source amplifier.

10. (Original) A phased array system in accordance with Claim 8, wherein said transmitter amplifier is a common source amplifier.

11. (Original) A phased array system in accordance with Claim 8, wherein said receiver amplifier further comprises a receiver electrode that is biased at a high voltage potential when

the receiver amplifier is in the receive mode.

12. (Original) A phased array system ain accordance with Claim 8, wherein said transmitter amplifier further comprises a transmitter electrode that is biased at a high voltage potential when the transmitter amplifier is in the transmit mode.

13. (Original) A phased array system in accordance with Claim 8, wherein said phased array system is one MMIC semiconductor wafer.

14. (Original) A phased array system in accordance with Claim 8, wherein said receiver amplifier further comprises interstage matching networks optimized for low noise figure and said transmitter amplifier further comprises interstage matching networks optimized for high power output.

15. (Previously presented) A phased array system in accordance with Claim 8, further comprising a combining matrix that has at least one matrix input port and at least one matrix output port wherein the first port of said at least one bi-directional amplifier is electrically connected to said at least one matrix input port.

16. (Original) A phased array system in accordance with Claim 15, wherein said at least one bi-directional amplifier is electrically connected to said at least one matrix output port said combining matrix.